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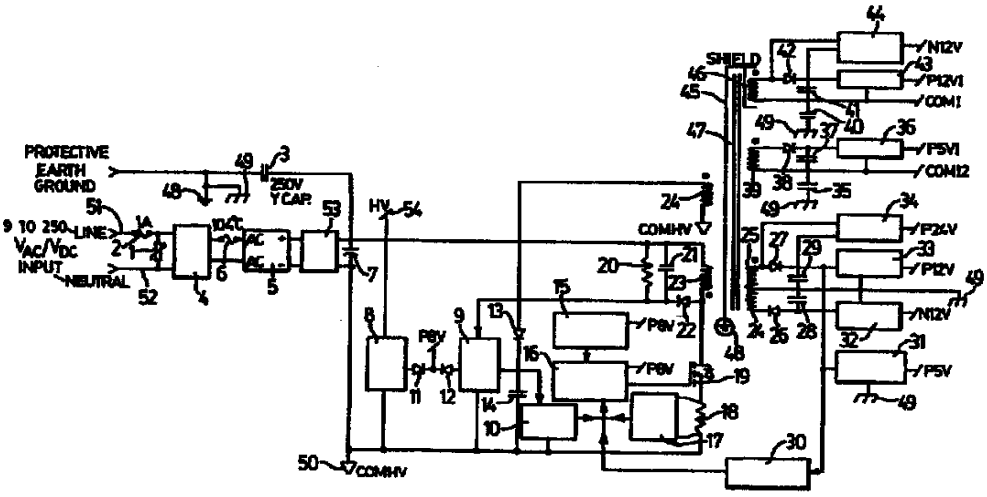
(54) Title: AN INTRINSICALLY SAFE UNIVERSAL SWITCHING POWER SUPPLY



(57) Abstract: A universal switching power supply for generating one or more output voltage levels wherein the power supply is operable over a range of AC and DC input supply voltages. The universal switching power supply achieves a ratio between the highest voltage and lowest voltage of at least 27. The universal switching power supply also features an intrinsically safe output. The intrinsically safe output circuitry comprises a PCB transformer.

WO 01/06631 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Title: **AN INTRINSICALLY SAFE UNIVERSAL SWITCHING POWER SUPPLY**

FIELD OF THE INVENTION

The present invention relates to universal switching power supplies, and more specifically to intrinsically safe universal switching power supplies. Intrinsically safe power supplies are particularly useful in petroleum and chemical industries.

BACKGROUND OF THE INVENTION

Switching power supplies are commonly used throughout the world in computers and many other apparatus. They are used because, for the same output power, they are much smaller and lighter. Switching power supplies also provide a good regulation of the outputs over a quite good range of input voltage. Isolated 90 to 250 Vac switching power supplies are quite common in the art. Isolated DC to DC switching power supplies with an input voltage range of 9 to 35 V are also quite common in the art.

Over the world, there are many voltage standards employed for powering electrical equipment. For instance, there are 9 Vac/Vdc, 12 Vac/Vdc, 24 Vac/Vdc, 48 Vdc/Vac, 90-250 Vac and sometime 129 Vdc. In addition, there are probably many other very special cases used around the world. So the main problem remains to find a truly universal power supply that does 9-250 Vac and Vdc.

In some chemical and petroleum industries, there is a need for a very high level of safety to make sure that the output is well isolated and won't create any risk of

flame, explosion or shock hazard. Power supplies of this type are commonly referred to as intrinsically safe (I.S.) power supplies. In fact, most of the time, only one of the power supply outputs is considered I.S.

To build an I.S. transformer, the transformer must have a large spacing with redundant protections to allow two faults anytime and anywhere in the power supply electronic circuit. With a normal frequency transformer, huge spacing is achieved by using separate bobbins on the same core. But when building a switching power supply, a high switching frequency must be used. This also means a much smaller inductance on each winding. To achieve a small inductance, the entire transformer is forced to be much smaller, and thus such a large spacing is almost impossible even with separate bobbins.

Accordingly, there remains a need for an intrinsically safe universal switching power supply.

BRIEF SUMMARY OF THE INVENTION

The present invention provides an intrinsically safe switching power supply able to cover 9-250 Vac, 40-70 Hz and 9-250 Vdc on the same power cord. The power supply provides outputs of -12V, +5V, +12V, +24V all referred to the earth ground. These voltages are available for digital and analog circuit purposes. Preferably, the power supply also generates an isolated 5V for RS-485 communication applications. The -12V and +12V outputs include an intrinsically safe isolation for an I.S. milliamp output circuit. All the rails are isolated from the input voltage.

To obtain an isolated output having huge spacing according to CENELEC standards (EN 50020) and to comply with

the international safety standard (IEC 1010-1) to get CSA and FM approvals. The switching power supply according to the present invention includes a multi-layer PCB, and the required spacings are obtained by keeping all windings inside the board. Advantageously, the core may comprise a standard planar core.

According to another aspect of the invention, a very wide range of voltages is obtained by producing very narrow pulses to control the MOSFET that switches the transformer. In a conventional switching power supply, the ratio between the highest voltage and the lowest voltage gives usually around 4 to 5 at the maximum. It is pretty rare to get a higher ratio than that. In the universal power supply of the present invention, the ratio is in fact over 27.7 (if we look at the 9 to 250 Volt range) up to 51. The voltage range is 7.2 Vdc to 387.5 Vdc if we consider the 1.4-Volt drop in the rectifier bridge and if we consider that the highest dc voltage is reached when the 250 Vac+10% voltage is rectified and provides 387.5 Vdc. So, one of the Intrinsically Safe Universal Switching Power characteristics is that the voltage ratio is obviously 10 times bigger than any other conventional switching power supply. The other characteristic is the PCB transformer used to get an I.S. output.

The power supply according to the present invention includes the following features:

(1) an alternating and direct current capability (ac/dc).

(2) the input voltage range is fully controlled by the electronics for the full ac/dc range and is transparent to the user, without the need for a manual voltage range selecting switch.

(3) the maximum input voltage and the minimum input voltage ratio gives a factor equal or greater than 7.3.

(4) a fly-back (step-up) topology.

(5) a duty cycle controller capable of providing 10ns to 7us pulse outputs.

(6) circuitry for creating the equivalent of a very low impedance MOSFET transistor at low voltage and a quick low stray capacitance MOSFET transistor at high voltage.

(7) at least one intrinsically safe voltage output comprising a PCB transformer and a planar core.

BRIEF DESCRIPTION OF THE DRAWINGS

Reference will now be to the accompanying drawings, which show by way of example, preferred embodiments of the present invention, and in which:

Fig. 1 shows in diagrammatic form an intrinsically safe universal power supply according to the present invention;

Fig. 2 is a diagrammatic view a transformer arrangement for the power supply of Fig. 1;

Fig. 3 is a graph showing the relative permeability as a function of the frequency;

Fig. 4 is a graph showing the maximum energy as a function of air-gap;

Fig. 5 is a cross-sectional view of the layers in a transformer printed circuit board (PCB) according to the invention;

Fig. 6 is a diagrammatic view of the first layer for the transformer PCB;

Fig. 7 is a diagrammatic view of the top layer of the transformer PCB;

Fig. 8 is a diagrammatic view of the intrinsically safe (I.S.) shielding layer of the transformer PCB;

Fig. 9 is a diagrammatic view of the low voltage side I.S. output secondary layer of the transformer PCB;

Fig. 10 is a diagrammatic view of the low voltage side P12V output secondary of the transformer PCB;

Fig. 11 is a diagrammatic view of the low voltage side N12V output secondary layer of the transformer PCB;

Fig. 12 is a diagrammatic view of the low voltage side P5VI output secondary layer of the transformer PCB;

Fig. 13 is a diagrammatic view of the GND layer for the transformer PCB;

Fig. 14 is a diagrammatic view of the high voltage side primary for the transformer PCB;

Fig. 15 is a diagrammatic view of the high voltage P8V output secondary for the transformer PCB;

Fig. 16 is a diagrammatic view of the bottom of layer 10 for the transformer PCB;

Fig. 17 is a schematic of the PCB transformer;

Fig. 18 is a general timing diagram;

Fig. 19 is a timing diagram for the oscillator and duty cycle controller;

Fig. 20 is a schematic showing the duty cycle controller for the power supply; and

Fig. 21 is a schematic showing the high voltage side of the power supply.

DETAILED DESCRIPTION OF THE INVENTION

Reference is first made to Fig. 1 which shows in block diagram form an intrinsically safe universal switching power supply according to the present invention. A 9 to 250 Vac/Vdc voltage is applied on line (51) and neutral (52) to feed the power supply. A protective earth ground (48) is provided for safety and for filtering. Preferably, the protective earth ground is able to withstand 30 amperes at any point. To be considered an intrinsically safe ground, it is also made with 1 oz. copper on the multi-layer printed circuit board (PCB). If an ac voltage is applied, it must be between 40 to 70 Hertz.

A 1-ampere fuse (2) with a minimum of 4000 Amperes of rupture capability is provided to protect the whole circuit. A varistor (1) is provided to protect the circuit against a 2000-Volt & 2-Ω surge. This is an EMC requirement to get the CE marking. The ac/dc voltage is then filtered with a filter (4) to reject the common mode noise generated by the switching. This is another EMC requirement to get the CE marking. A 104°C thermal fuse (6 & 55) is connected before the rectifier bridge. It is preferable to install the thermal fuse in this location since it is physically sitting

under the PCB transformer (see 55) and can pick up a high frequency noise. This noise will be filtered by the common mode choke in the filter (4). It would not have been filtered if the thermal fuse had been the other side of the filter.

The ac/dc voltage is rectified by a diode bridge (5) and is filtered by a high frequency filter preferably made with a COG ceramic capacitor and a ferrite bead. This filter is especially made to filter the noise over 50 MHz created by the switching. A low impedance, low value capacitor (7) is connected at the output of the filter (53) to remove some ripple at the output of the bridge. The goal of the capacitor (7) is not to get a pure dc voltage with no ripple (in any case, it would not achieve that kind of goal at low ac voltage.). Its unique goal is to provide a source of current for the high peak of current created by switching the primary of the transformer (23).

Of course, to switch a transistor (19) at high frequency, a high frequency oscillator and a controller that will modify the switching duty cycle are needed. Since a MOSFET transistor gate has a Vgs = 4 Volts and needs about 8 Volts to really turn on, the voltage needs to be generated from the high voltage side (54). The HV voltage (54) can be as low as 6.8 Volts when the input voltage is 8.2 Volts and as high as 400 Volts when a high ac voltage is applied at the input. For this reason, linear regulator (8) is made directly from the HV voltage. As the oscillator (15) and the controller (16) may consume up to 10 mA at high voltage, the dissipation into the linear regulator could be as high as 4 Watts. That's a lot and not acceptable. Thus, the linear regulator (8) is only used as a start-up circuit and another more efficient 8 Volts is generated from the switching

transformer (24). It is preferable to start up the circuit with 5.5 Volts with the regulator (8) and generate about 10 Volts across the capacitor (14) from the secondary (24). This 10 Volts is then regulated to around 8 Volts from the regulator (9). Because of the two diodes (11) and (12), as soon as the power supply begins to generate a higher voltage than 5.5 Volts, the regulator (8) is disabled. At that point, it no longer dissipates anything. If for some reason the switching power supply was not able to start up properly, the regulator (8) would blow up almost instantaneously.

The oscillator (15) generates a 100 kHz, 70% duty cycle square wave. This 70% duty cycle is basically the maximum duty cycle allowed by the controller (16). A change in that duty cycle would change the maximum duty cycle allowed by the controller (16). 100 kHz is selected as basic frequency because it is more than twice the switching frequency of other oscillators in our products (we use often 44 kHz for ultrasonic equipment). It is not desirable to generate a frequency that could be picked up by the receivers. At 7.6 Vdc of input voltage, the MOSFET transistor (10) time on duration is around 4.4μs. At 387.5 Vdc it is 86 ns. If the circuit load decreased by 1/10, the time on could be as short as 8.6 ns at 387.5 Vdc. It means that the transistor (19) must switch very fast and the controller has to be able to produce very narrow pulses. Typically, a controller is able to generate a ramp up & ramp down of 4 ns or less.

For the values:

V_{min}=7.6 Vdc The 7.6 Vdc comes from 7.6*Vdc*=9*Vdc* (Voltage drop in the bridge (5))

V_{max}=387.5 Vdc The 400 Vdc comes from (275Vac*$\sqrt{2}$) - 1.4*Vdc*=387.5*Vdc*

F=100 kHz Switching frequency.

First the inductance of the transformer primary (23) must be determined. To be able to do that, the configuration of the output and the load on each secondary winding will be able to calculate the output power needs to be known. A table of the different voltages on each rail with their respective current and power consumption is provided as follows:

Name of rail	# of turn	Real produced voltage	Current on rail	Power dissipation calculation (Dissipation from the winding point of view)
P24V	-	25.18	Not used	Not used
P12V	10	13.14	0.080	P=13.14 * 0.080 = 1.051
P5V	-	5.0	0.120	P=(5.0*0.120)/0.90=0.667
N12V	10	-13.14	- 0.050	P=-13.14 * -0.050=0.657
P5V1	4	5.256	0.045	P=5.256 * 0.045=0.237
P12VI	10	13.14	0.030	P=13.14 * 0.030=0.394
N12VI	-	-12.04	- 0.030	P=(-12.04-0.7-2*0.2)*-0.030=0.394
P8V	8	7.7	0.01	P=10.512 * 0.01=0.105
				Total power = 3.505 Watts

It will be appreciated that there are n turns for the P5V, P24V & N12VI. It is because these voltages are obtained by other methods as switching capacitors or switching integrated circuits. The 24V is not used and it is there only for future requirement. It will not be considered in the present power consumption. If the 24 voltage is used, the whole calculation of the primary inductance (24) will be affected and should be redone.

To calculate the peak current in the primary inductance (24) and the value of that inductance itself:

$V = \frac{(*dI)}{dt}$ Voltage across an inductance in general

$F = \frac{1}{t_{on} + t_{off}}$ Frequency at 9 Vdc (Not true at higher voltage)

$E = \frac{1}{2} * L * I^2$ Energy stored in the magnetic field

$L = N^2 * A_L$ Inductance value calculation

$L_T = L_1 + L_2 + L_3 + L_4 + L_5$ Total inductance

With the previous formulae and with some mathematical manipulations, the following is found:

$$I_p = 2 * P_{out} * \left[\frac{1}{V_{\min}} + \left[\left(\frac{N_{s1}}{N_p * V_1} \right) + \left(\frac{N_{s2}}{N_p * V_2} \right) + \left(\frac{N_{s3}}{N_p * V_3} \right) + \left(\frac{N_{s4}}{N_p * V_4} \right) + \left(\frac{N_{s5}}{N_p * V_5} \right) \right] \right]$$

$$L = \frac{1}{F * I_p * \left[\frac{1}{V_{\min}} + \left[\left(\frac{N_{s1}}{N_p * V_1}\right) + \left(\frac{N_{s2}}{N_p * V_2}\right) + \left(\frac{N_{s3}}{N_p * V_3}\right) + \left(\frac{N_{s4}}{N_p * V_4}\right) + \left(\frac{N_{s5}}{N_p * V_5}\right)\right]\right]}$$

With the specific input/output voltages and the consumption of each output to be achieved, the following values are found:

$I_p = 2.096 Amperes$

$L = 16 \mu H$

With a 72% average efficiency in fly-back power supplies, a total power consumption of 4.87 Watts at the input of the product can be expected.

The Philips company is doing planar cores for planar transformers. Planar transformers is a new technology using PCB tracks as windings. There are different materials existing. A material able to work from 100kHz up to 5.8 MHz in a regular 9-250 Vac/Vdc application is selected. This wide frequency response is required to produce the large 4.4-us pulses at 7.6 V and the 86-ns narrow pulses at 387.5 Vdc. In the present embodiment, the 3F3 material is used to achieve that wide frequency range (see Figure 3). Advantageously, it provides low cost, low loss, and gives a good frequency response.

Philips produces different core sizes. It has been found that the minimum size requirement to fit all windings is a 32 mm core (in the E32/6/20 series). Fitting all windings in a core is not all. It must be ensured that the core is able to transfer the energy. Philips supplies a graph of the energy(L^*I^2) as a function of the air-gap for a 3F3 E32/6/20 core (see Figure 4). To get a 16μH inductor, a 1.2-mm air-gap in a 3F3 E32/6/20 core is needed. For I_p=2,096 Amperes and for a 16μH inductor, we get L^*I^2=70uJ. On the Figure 4), it was found that a 1.2-mm air-gap yields 9mJ=9000 uJ. It is 128 time more than needed. In our application, it is perfectly acceptable to use a 3F3 core in the E32/6/20 series; it is big enough to meet the minimum physical requirement and the maximum energy requirement.

In Figure 2) a 3 dimensional view of the PCB transformer construction is shown. It is mainly made with a planar core (57), a 10-layer PCB (56), a bit of silicon glue (65), a Kepton tape (58), a thermal fuse (55) and two connectors (162) & (163). The planar core (57) is made with 3F3 material E-Core (63) and a 3F3 material plate (66). Accordingly to the CENELEC standard (EN 50020), it is necessary to wave solder the two connectors (162) & (163) and the thermal fuse (55). This is to provide reliable connections between the power supply board and the transformer PCB (56). The E-core (63) is glued on the PCB (56) with a bit of silicon glue (65). This is necessary to fill the gap between the board and the core and to pass the vibration test. It is not necessary to glue the plate (66) with the PCB (56) since it is well tied together with a Kepton tape (58).

The thermal fuse (55) sits under the transformer. In reality, once the PCB transformer is installed on the main

power supply board, a big 22μF, 400V electrolytic capacitor (see C12 on Figure 21) also sits under the PCB transformer. The thermal fuse (55) becomes sensitive to the heat generated by the 10-layer PCB (56) and also to the heat generated by the C12 capacitor. C12 is a 105°C capacitor. The 10-layer PCB (56) is rated for 130°C. The Curie temperature of the planar core (57) is over 200°C. So, in this construction, the weakest component is the C12 capacitor. Because of its 105°C rating, a 104°C thermal fuse (55) is selected. The thermal fuse manufacturer specifies that the fuse will blow up under 104°C but never over.

Fig. 5 shows in detail a cross section of the 10-layer PCB transformer. The whole PCB is made with four cores separated with five prepeg layers. The top (layer 1) and bottom (layer 10) are made with a 1 Oz copper foil plated with ½ Oz tin. It is important to note that according to the CENELEC standard (EN 50020), all intrinsically safe shield or guard must have at least 1 Oz of copper. Tin plating does not count in that thickness.

Fig. 6 shows the PCB transformer silkscreen. It is important to have no silkscreen in the planar core area. The thickness of the board is very tight there. It is noted that the total thickness of the board is 0.1145" +/- 10%. But in the core area, as there is no copper on top and bottom of the board, we have only 0.1103" +/- 10%. Philips specify a free room of 0.1252" +/- 0.0079" between the E-core (63) and the plate (66). As a result, there is a potential conflict. The PCB may have as thick as 0.1213" and the core may have only 0.1173" of room. In that situation, the air-gap (that is already 1.2mm) would be increased by 0.0004" (0.1mm). This is a rare situation which will not typically be a problem. The inductance will vary a bit but not enough

to create a real problem. However, preferably the production test procedure will catch any transformer that causes a problem.

Figs. 7 to 16 show the artwork of each layer in a 3:1 scale. The spacing requirements for the different approval agencies are provided as follows:

In red denoted by (a), the minimum required spacing and requirements to get an intrinsically safe out (EN 50020 CENELEC standard). The following is a summary of the rules applied (see EN 50020 standard for more details):

- The distance through isolation between the I.S. winding and all other windings is at least 1 millimetre.

- The distance through isolation between the I.S. winding and the I.S. earth ground is at least 0.5 millimetre.

- The distance on the surface of the board between the I.S. winding and all other windings is at least 10 millimetres.

- The distance on the surface of the board between the I.S. winding and the I.S. earth ground is at least 2 millimetres.

- The distance through air between the I.S. winding and all other windings is at least 6 millimetres.

- The thickness of all I.S. earth ground shields and I.S. grounded guards is at least 1 oz. copper.

- The width of all I.S. grounded guards is at least 2 millimetres.

- In case of a fault, the temperature of windings cannot reach the Curie temperature of the core transformer and cannot reach the temperature specification of the PCB material.

- A thermal fuse connected in series with the main power must be mounted on the PCB transformer to prevent any damage to the PCB isolation if ever there is a failure somewhere in the power supply.

- Two independent pins bring the earth ground to the PCB to provide what we call the I.S. earth ground.

- A wave-soldering machine is used to solder the connectors (a manual soldering is forbidden).

- A safe I.S. output must be provided even if there is two faults (please see the EN 50020 standard to know what this means).

- The I.S. output must pass successfully the Hipot test.

In green denoted by (b), all the minimum required spacing and requirements to pass the CSA & FM general safety approvals (International IEC 1010-1 standard) are provided. The following is a summary of the rules applied (see IEC 1010-1 standard for more details):

- The distance through isolation between any accessible windings and high voltage is at least 0.4 millimetre.

- The distance through isolation between high voltage and protective earth ground is minimum.

- The distance on the surface of the board between any accessible windings and high voltage is 3.3 millimetre or two times 1.5mm.

- A protective ground must be able to withstand 30 Amperes during one minute.

- The high voltage windings and all accessible outputs must pass successfully the Hipot test.

In blue denoted as (c), all the minimum required spacing and requirements to pass the 4000Vp common mode surge test (EMC requirement) an intrinsically safe output (EN 50020 CENELEC requirements) are provided. The following is the list of rules applied:

- The CENELEC safety agency does not give the right to connect any varistor between the neutral and ground to pass the EMC "Surge" test (4000VP in common mode). Therefore, we are obliged to keep at least 4 millimetres in air and on the surface of the board between the high voltage and any earth ground and secondary windings. By high voltage we understand all windings connected directly or indirectly to the main power source without a galvanic isolation.

From the switching point of view now, MOSFET transistors are used because of their very fact switching time and because of their high voltage capabilities. Unfortunately, a MOSFET transistor having high current capabilities will also have very high stray capacitance. It is even higher with heavy loads since the gate stray capacitance is multiplied by the Miller effect. On the other hand, high current is only found at low voltage and at that time, a fast transistor is not really necessary. Therefore, at low voltage, a huge stray capacitance is tolerable.

For high voltage, a very quick MOSFET with a very low gate stray capacitance is needed. At that time, it is necessary to sacrifice the high current capabilities and trade it for a low gate stray capacitance MOSFET. At high voltage, the generated pulse width is very narrow (may be less than 10ns). As a result the MOSFET gate needs to be charged and discharged very quickly.

As will be appreciated, it is difficult to find a good compromise to reduce the thermal loses. A solution is shown on the Fig. 20. Two MOSFET transistors (107) and (109) are used instead of only one. The two sources together and the two drains together are tied together. The gates are connected together via a resistor (105) and a fast recovery diode (106).

At low voltage, the pulse generated in (104) is quite large. The current slowly ramps up linearly through the transformer primary inductance (110). This means that in the first few microseconds, the current through the MOSFET drains is pretty low. The MOSFET gate (108) has plenty of time to charge up and when the current becomes high through the drains, the two MOSFET transistors are really in

parallel. They are sharing evenly the current and they are reducing the thermal losses due to high current. The diode (106) discharges quickly the two gates in same time.

At high voltage, the MOSFET gate (108) cannot charge enough to turn on properly the transistor. As the major stray capacitance is due to the Miller effect, the total stray capacitance viewed from the drain is half the value of what it would have been if the two MOSFET transistor were connected in parallel. Therefore, the equivalent of a high frequency MOSFET transistor with a low high frequency loss is obtained.

In conclusion, the best of a high frequency MOSFET transistor and the best of a low impedance, high current capabilities MOSFET transistor are achieved.

In order to obtain a huge input voltage range, a very fast controller is required. Most of modern ICs are using TTL or CMOS technologies. The push-pull configuration is one of the fastest ones on the market. Unfortunately, each transition consumes a lot of current since for a brief moment, two transistors are making a short circuit between the Vcc and the ground. If just one transistor is used and a resistor as pull-up or pull-down, one fast edge is obtained, but a very slow complementary one. The peak current is reduced considerably, but the average current is increased. With just a transistor-resistor combination, it would be impossible to create a 10ns pulse width. But if there are two waveforms (one with fast rise time and a falling time and another one with a slow rise time and a fast falling time) a very narrow pulse could be created by shifting one waveform in reference to the other. The two waveforms are inputted to an AND gate circuit and a variable

duty cycle square weave (with sharp edges) is created. Of course, the AND gate circuit must be a very quick one.

As shown in Fig. 20, there is a 70% duty cycle 100kHz oscillator (76). It generates the waveform (67) in Figure 19). The oscillator duty cycle imposes the maximum limit of the final duty cycle at the output in (104). This way, the condition where the two MOSFET transistors (107 & 109) would be on all the time (and making a total short circuit) is blocked.

The oscillator output (77) passes through a first circuit (136) with two inverter gates (78 & 80) providing two complementary signals (79 & 81).

The circuit (82) creates a fixed duty-cycle waveform with a very quick rising time (less than 4ns) and a slow falling time (see (69) in Fig. 19).

The circuit (83) creates a variable duty-cycle waveform with a slow rising time and a very fast falling time (less than 4 ns). It slowly ramps up (70 or 72 or 74) before the waveform (69) and very quickly fall down sometime after when the waveform (69) is still high level. It can create a very narrow pulse (8ns large in (70)) or a wide pulse (in (73) and (75)) with very sharp edges.

The circuit (129) generates a variable duty cycle waveform that is controlled by a feedback (126). Basically, a capacitor (133) is charged and discharged to obtain the waveform (68) in (134). As soon as the voltage across that capacitor reach a level determined by the feedback input (126), it turns on the transistor (132). Depending on the Feedback2 level (126), the pulse width varies. It is around

8ns when Feedback2 is 0 Volt and it is around 7μs when Feedback2 is 8 Volts.

The transistor (91) in series with (124) forms an AND circuit. This AND circuit has a very quick rise time since the transistor (90) is already on when the transistor (124) turns on. It also has a very quick falling time since the transistor (91) is a follower and has almost no stray capacitance to discharge. The output (94) is also forced to fall down very quickly by using a Schottky diode (92). To obtain a very powerful inverter gate (89) four gates are placed in parallel (not shown in Fig. 20).

The circuit (122) is in fact a very fast and powerful buffer. It charges up and discharges the two MOSFET gates.

For safety, any over current spikes are detected by a low impedance 4-wire resistor (in fact, it is made with a PCB track). If ever any current above a certain threshold was detected, it would shut down the power supply by reducing the Feedback2 level (126) to the minimum (0 Volt). After a fraction of second, the Feedback2 level is authorized to rise again. If ever another over current level is detected, the power supply will shut down again. Even if a fault condition is maintained, and even if the power supply tries to restart every second, the energy involved is very low and nothing that would damage the power supply happens.

Fig. 18 shows different timing curves. As we can see the waveform generated at the transformer output is like (157). The upper side of the waveform (161) is always the same height but the bottom side is able to go very low in negative voltage. The rectifiers keep only the upper side

of this waveform and with capacitors, the output voltages (162) are filtered. Of course each output has its own voltage and are represented by Vcc in Fig. 18.

Figs. 20 and 21 show the real schematic of the electronic circuit. Fig. 20 shows the high voltage side with the oscillator, the controller, the MOSFET transistor switches, etc. The Fig. 21 shows all outputs.

WHAT IS CLAIMED IS:

1. The switching power supply as substantially described herein.

2. The switching power supply as substantially depicted herein.

3. The method for operating the switching power supply as substantially described herein.

AMENDED CLAIMS

[received by the International Bureau on 14 November 2000 (14.11.00);
original claims1-3 replaced by amended claims 1-3
new claims 4-6 added; (4 pages)]

1. A switching power supply for generating one or more voltage outputs, and one of the voltage outputs comprising an intrinsically safe voltage output, said switching power supply comprising:

(a) an input stage having means for receiving a supply voltage and means for converting said voltage to a DC level;

(b) a first stage coupled to said input stage for receiving said DC level and said first stage having means for producing an output voltage from said DC level;

(c) a second stage coupled to said first stage and having means for receiving said output voltage produced by said first stage and including means for generating one or more voltage outputs and an intrinsically safe voltage output;

(d) means for isolating said second stage from said first stage comprising a planar core transformer;

(e) said first stage including primary windings electromagnetically coupled to said planar core transformer, and said primary windings comprising a plurality of conductive tracks formed on a layer of a multi-layer circuit board;

(f) said second stage including secondary windings electromagnetically coupled to said planar core transformer, and said secondary windings comprising a plurality of conductive tracks formed on another layer of said multi-layer circuit board, and said secondary windings including windings formed as a plurality of conductive tracks for generating said intrinsically safe voltage output, and said other layer being isolated from said layer carrying said conductive tracks for said primary windings.

2. An intrinsically safe switching power supply for generating one or more voltage outputs, said switching power supply comprising:

(a) a circuit board having a plurality of layers, and including an opening for receiving a transformer;

(a) a first stage having an input for receiving a supply voltage and including means for converting said supply voltage to a DC level and having circuitry for producing an output voltage from said DC level, and said first stage including primary windings, said primary windings being formed as conductive tracking on one layer of said circuit board;

(c) a second stage coupled to said first stage through said transformer and said second stage including secondary windings for coupling said output voltage produced by said first stage through said transformer, said second stage including circuitry for generating one or more voltage outputs, and said secondary windings being formed as conductive tracking on another layer of said circuit board, and said circuit board including an output layer for said voltage outputs;

(e) said second stage including a sub-stage for generating an intrinsically safe voltage output, and said sub-stage comprising a plurality of separate secondary windings for coupling said output voltage produced by said first stage and circuitry for generating said intrinsically safe voltage output, and said separate secondary windings comprising conductive tracking formed on another layer of said circuit board, and said layer carrying the conductive tracking for said intrinsically safe voltage output being isolated from said other layers in said circuit board.

3. The intrinsically safe switching power supply as claimed in claim 2, wherein said transformer stage comprises a planar core transformer, and said circuit board comprises a multi-layer printed circuit board, wherein said conductive tracking comprises electrically conductive printed circuit tracks.

4. The intrinsically safe switching power supply as claimed in claim 2, wherein said circuit board includes shield layer for shielding said layer carrying the secondary windings for said intrinsically safe voltage output, said shield layer being situated between said output layer and said layer carrying the secondary windings for said intrinsically safe voltage output.

5. The intrinsically safe switching power supply as claimed in claim 4, wherein said circuit board includes a ground layer for reducing stray capacitance, said ground layer being situated between the layer carrying said primary windings and the layers carrying said secondary windings.

6. A switching power supply for generating one or more voltage outputs, and one of the voltage outputs comprising an intrinsically safe voltage output, said switching power supply comprising:

(a) an input stage having means for receiving a supply voltage and means for converting said supply voltage a DC level input;

(b) a first stage coupled to said input stage for receiving said DC level and said first stage having means for producing an output voltage from said DC level;

(c) a second stage coupled to said first stage and having means for receiving said output voltage produced by

said first stage and including means for generating one or more voltage outputs and an intrinsically safe voltage output;

(d) means for isolating said second stage from said first stage comprising a planar core transformer;

(e) said first stage including primary windings electromagnetically coupled to said planar core transformer, and said primary windings comprising a plurality of conductive tracks formed on one layer in a multi-layer circuit board;

(f) said second stage including secondary windings electromagnetically coupled to said planar core transformer, and said secondary windings comprising a plurality of conductive tracks formed on one or more layers in the multi-layer circuit board;

(g) a start-up stage coupled to said first stage and said input stage, said start-up stage including means for starting said power supply during a low period.

STATEMENT UNDER ARTICLE 19(1)

The claims in the subject application have been amended to clarify the language and better distinguish the invention over the prior art.

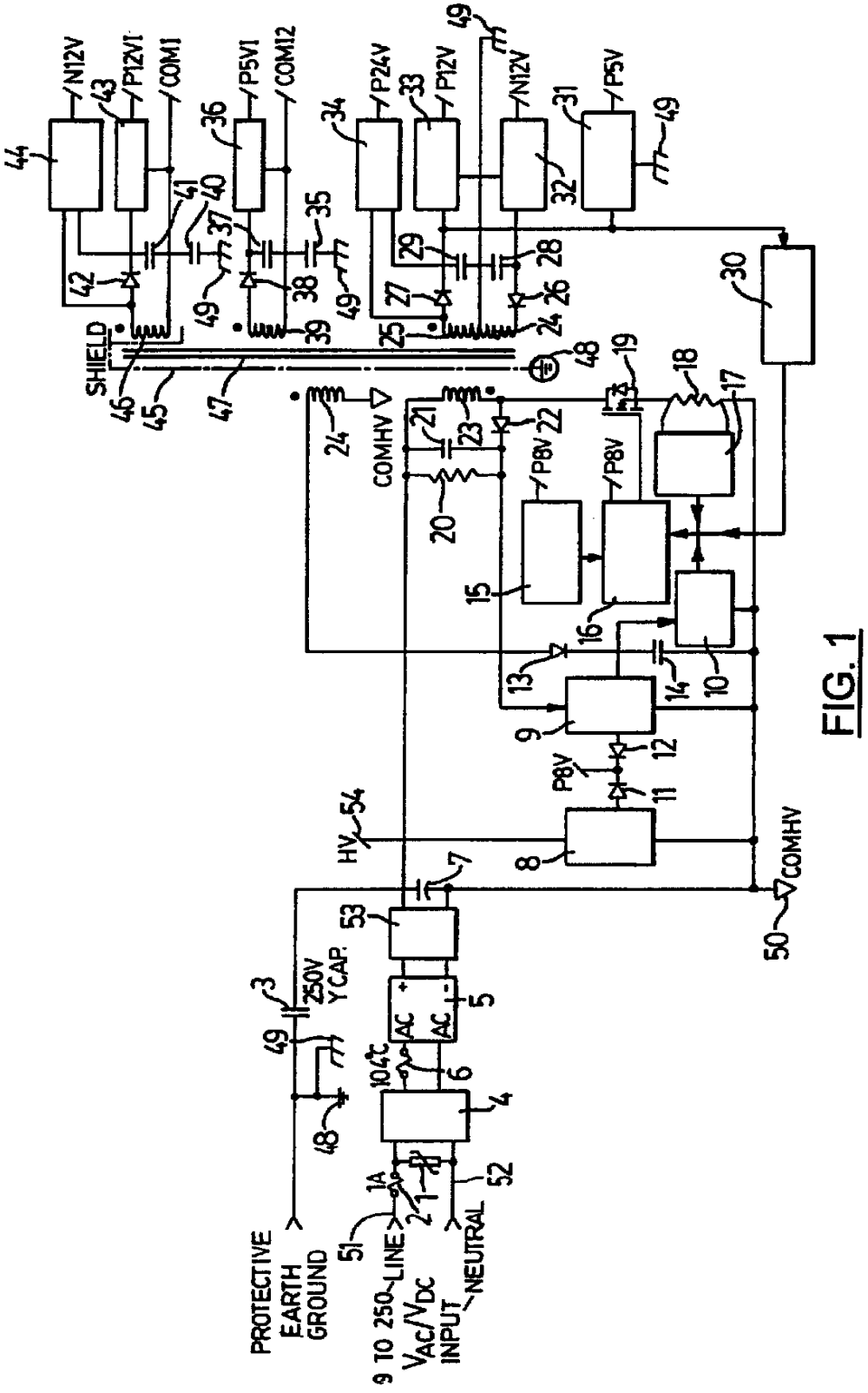

N12V
P12VI
COM1
P5V1
COM12
P24V
P12V
N12V
P5V
SHIELD
COMHV
P8V
HV
250V YCAP
AC
AC
PROTECTIVE EARTH GROUND
9 TO 250 VAC/VDC INPUT
LINE
NEUTRAL

FIG. 1

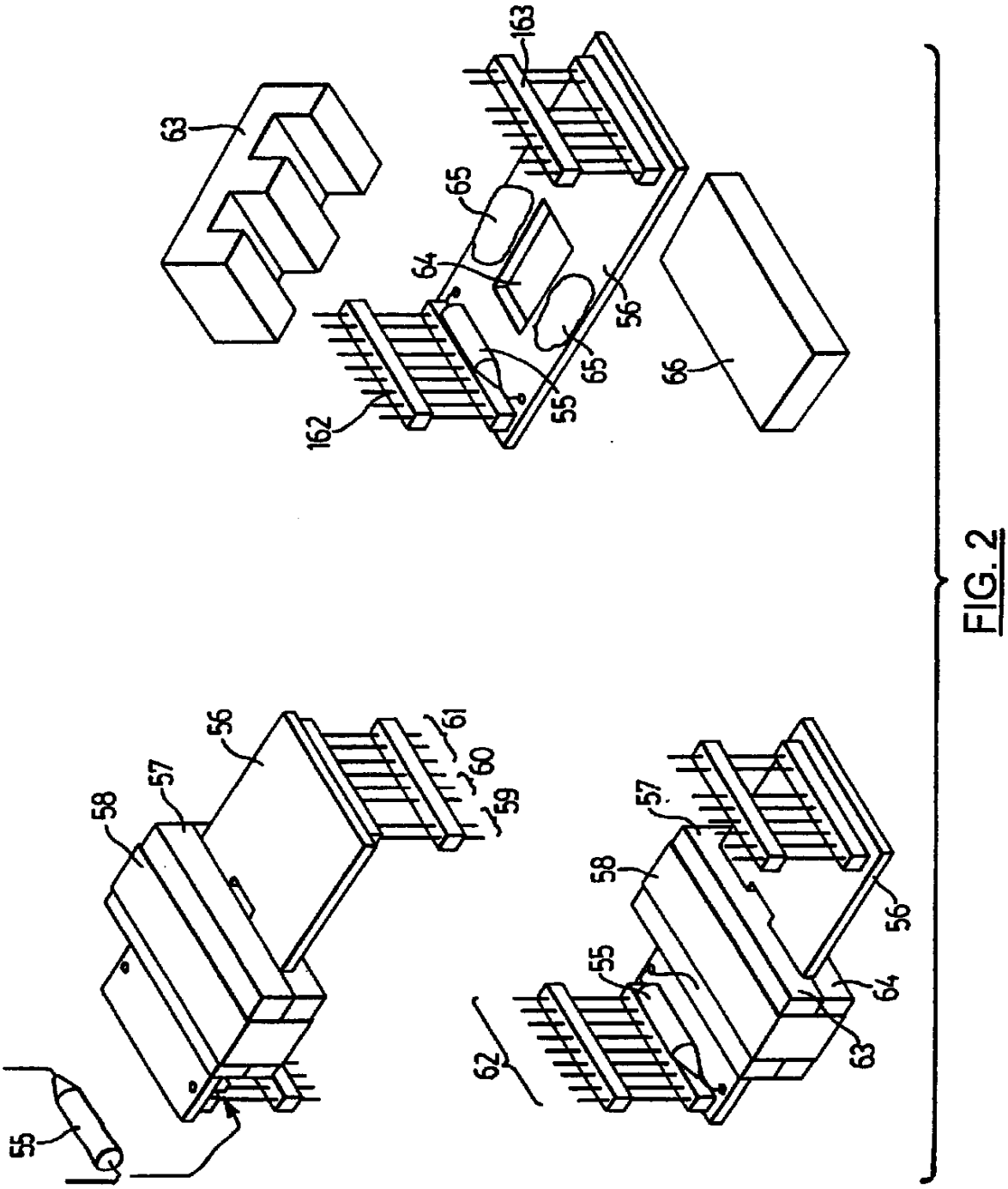


FIG. 2

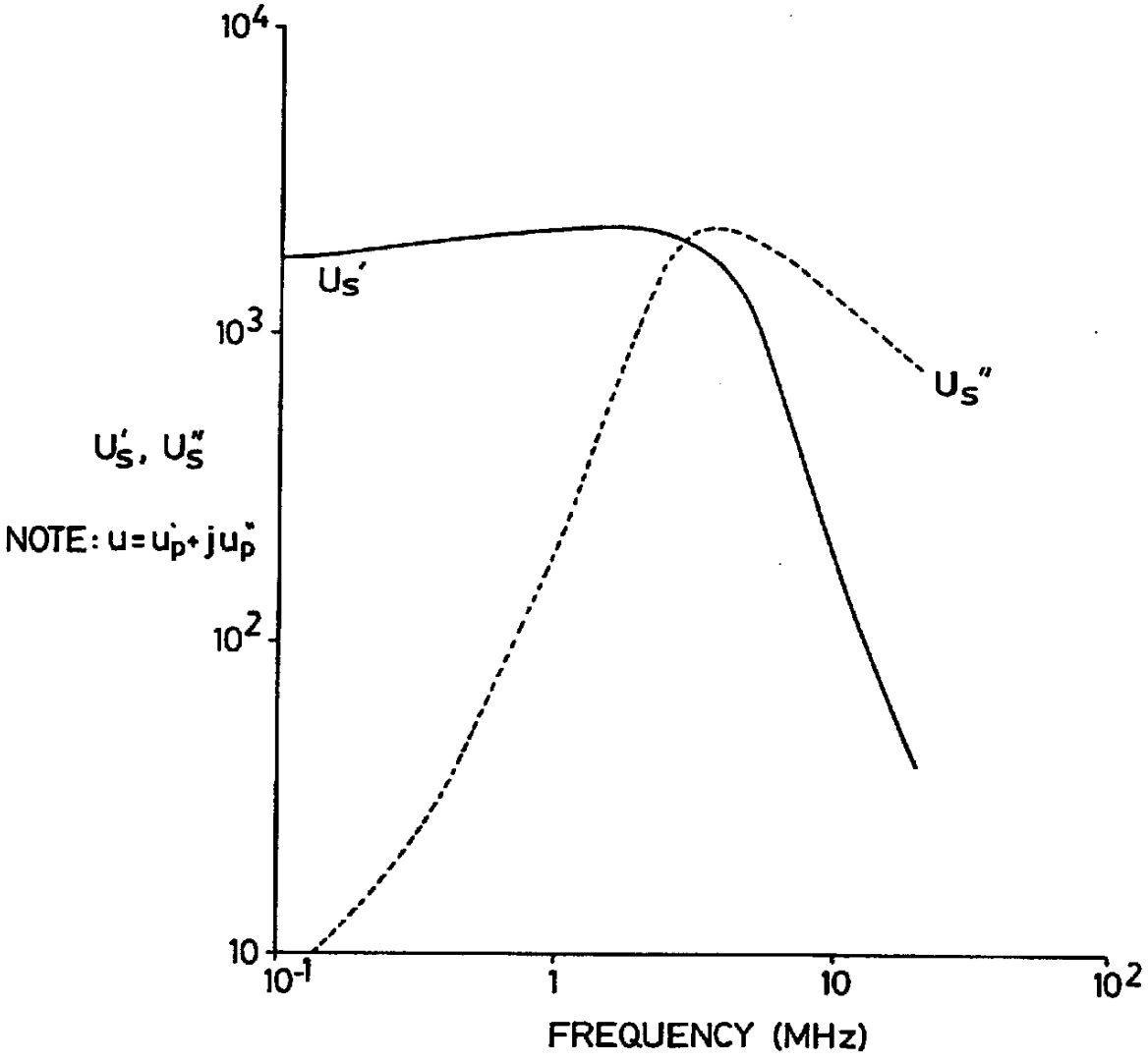

10^4
10^3
10^2
10
U_S'
U_S''
U_S', U_S''
NOTE: $u = u_p' + j u_p''$
10^{-1}
1
10
10^2
FREQUENCY (MHz)

FIG. 3

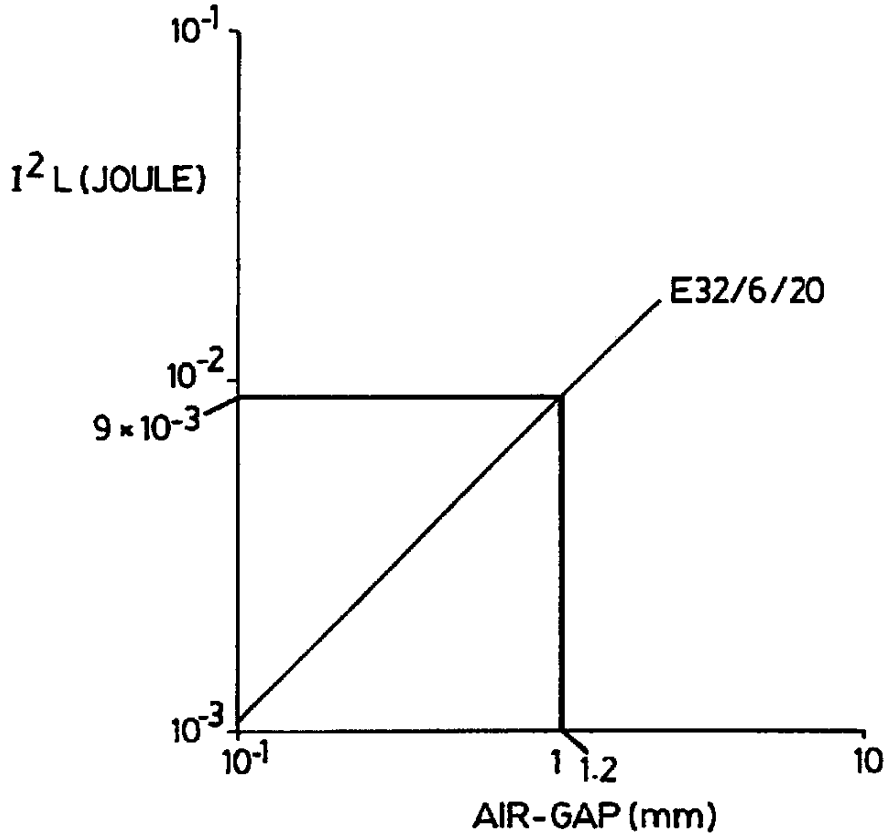


FIG. 4

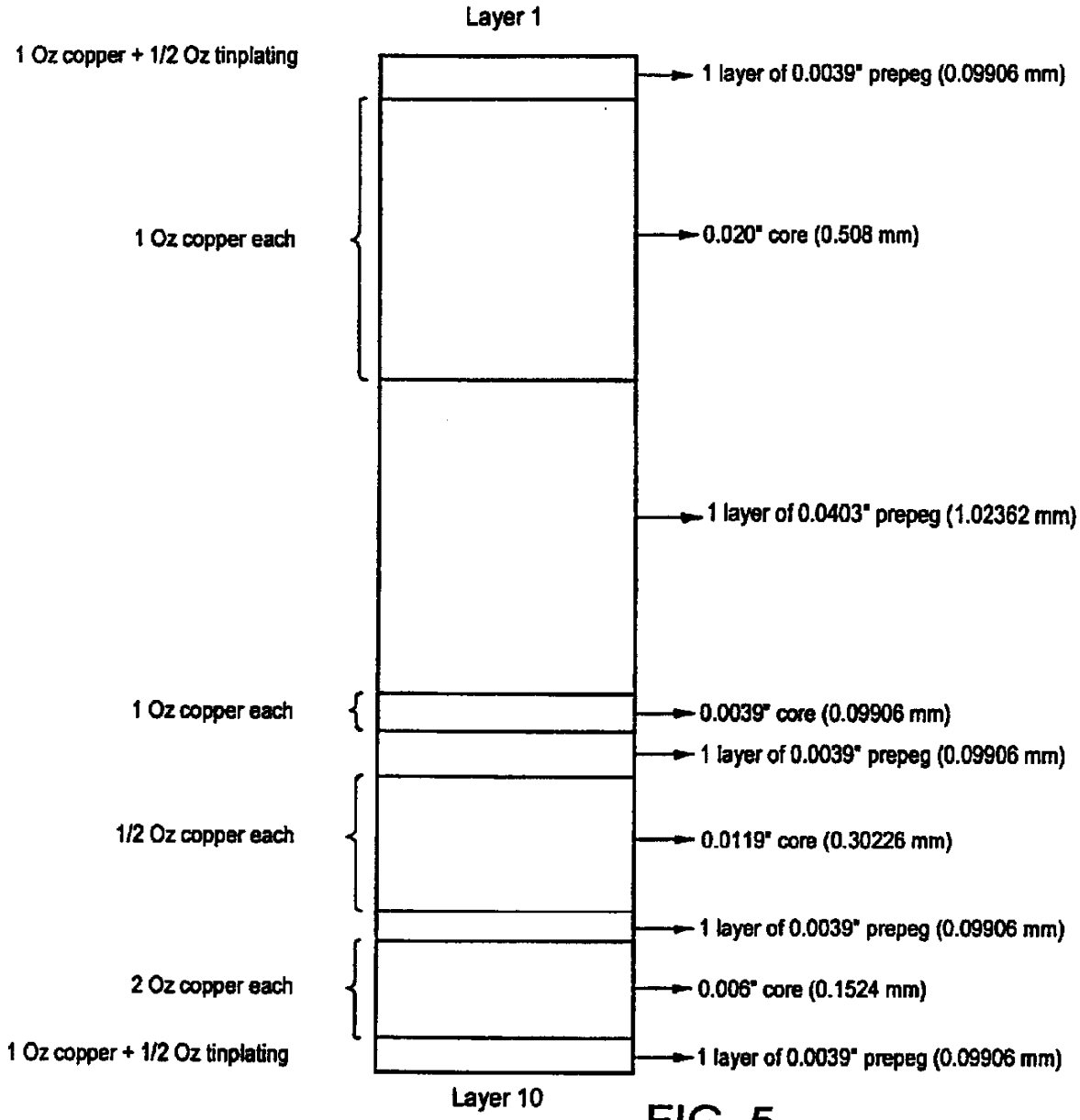


FIG. 5

TOTAL INSULATION =	0.0977" (2.48158 mm)
2 x 2 Oz COPPER LAYERS =	0.0056" (0.14224 mm)
6 x 1 Oz COPPER LAYERS =	0.0084" (0.21336 mm)
2 x 1/2 Oz COPPER LAYER =	0.0014" (0.03556 mm)
2 x 1/2 Oz TIN PLATING =	0.0014" (0.03556 mm)
TOTAL THICKNESS	0.1145" (2.9083 mm) +/- 10%
CORE AREA THICKNESS	0.1103" (2.8016 mm) +/- 10% (WITHOUT TOP & BOTTOM PLATED COPPER)

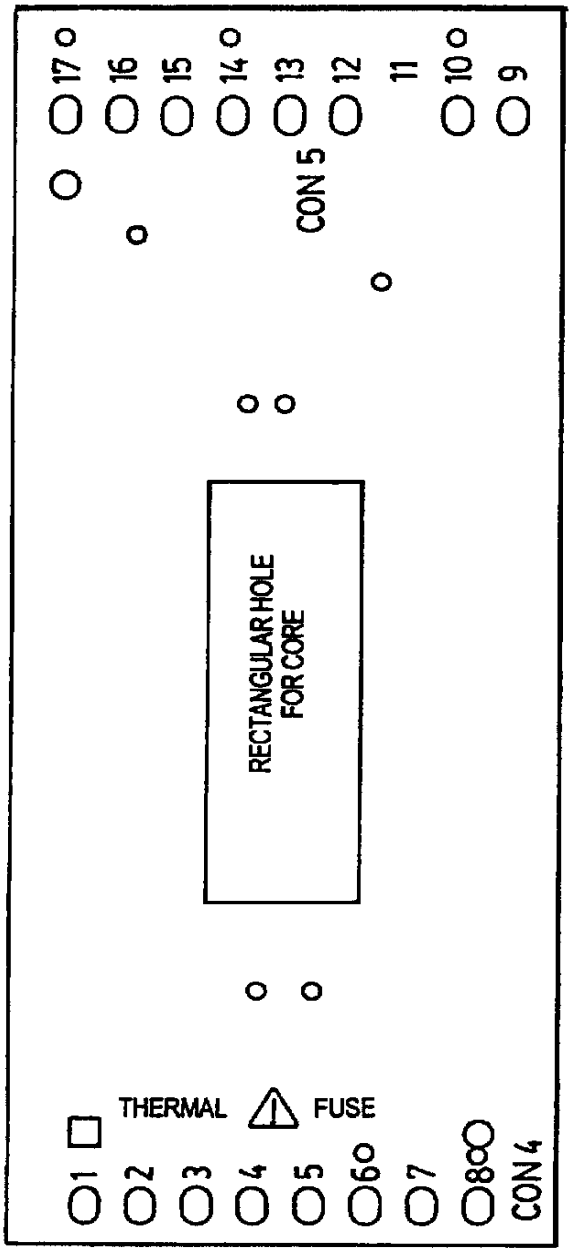

17
16
15
14
13
12
11
10
9
CON 5
RECTANGULAR HOLE FOR CORE
LAYER 1
THERMAL
FUSE
1
2
3
4
5
6
7
8
CON 4

FIG. 6

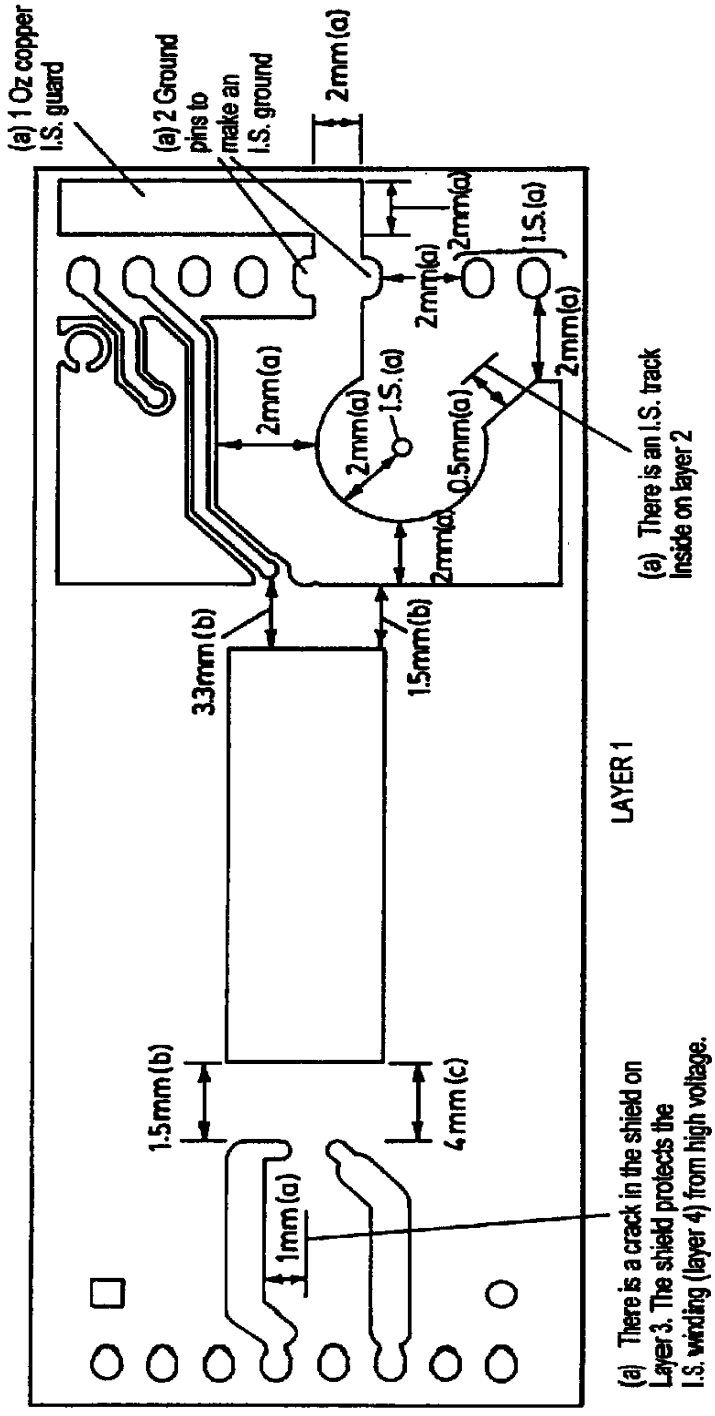

(a) 1 Oz copper I.S. guard
(a) 2 Ground pins to make an I.S. ground
2mm (a)
2mm(a)
I.S.(a)
2mm(a)
2mm(a)
2mm(a)
I.S. (a)
2mm(a)
0.5mm(a)
2mm(a)
(a) There is an I.S. track inside on layer 2
3.3mm (b)
1.5mm(b)
LAYER 1
1.5mm (b)
4mm (c)
1mm (a)
(a) There is a crack in the shield on Layer 3. The shield protects the I.S. winding (layer 4) from high voltage.

FIG. 7

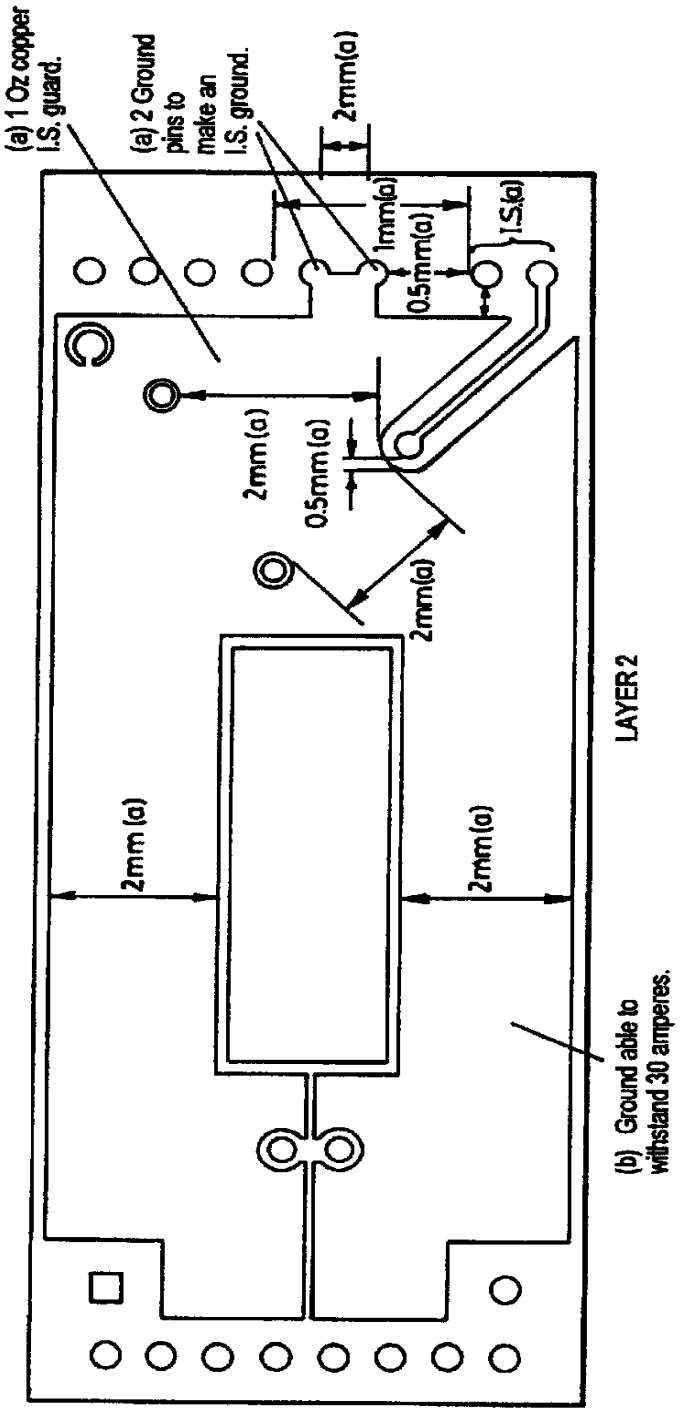

(a) 1 Oz copper I.S. guard.
(a) 2 Ground pins to make an I.S. ground.
2mm(a)
1mm(a)
0.5mm(a)
I.S.(a)
2mm(a)
0.5mm(a)
2mm(a)
2mm(a)
2mm(a)
LAYER 2
(b) Ground able to withstand 30 amperes.

FIG. 8

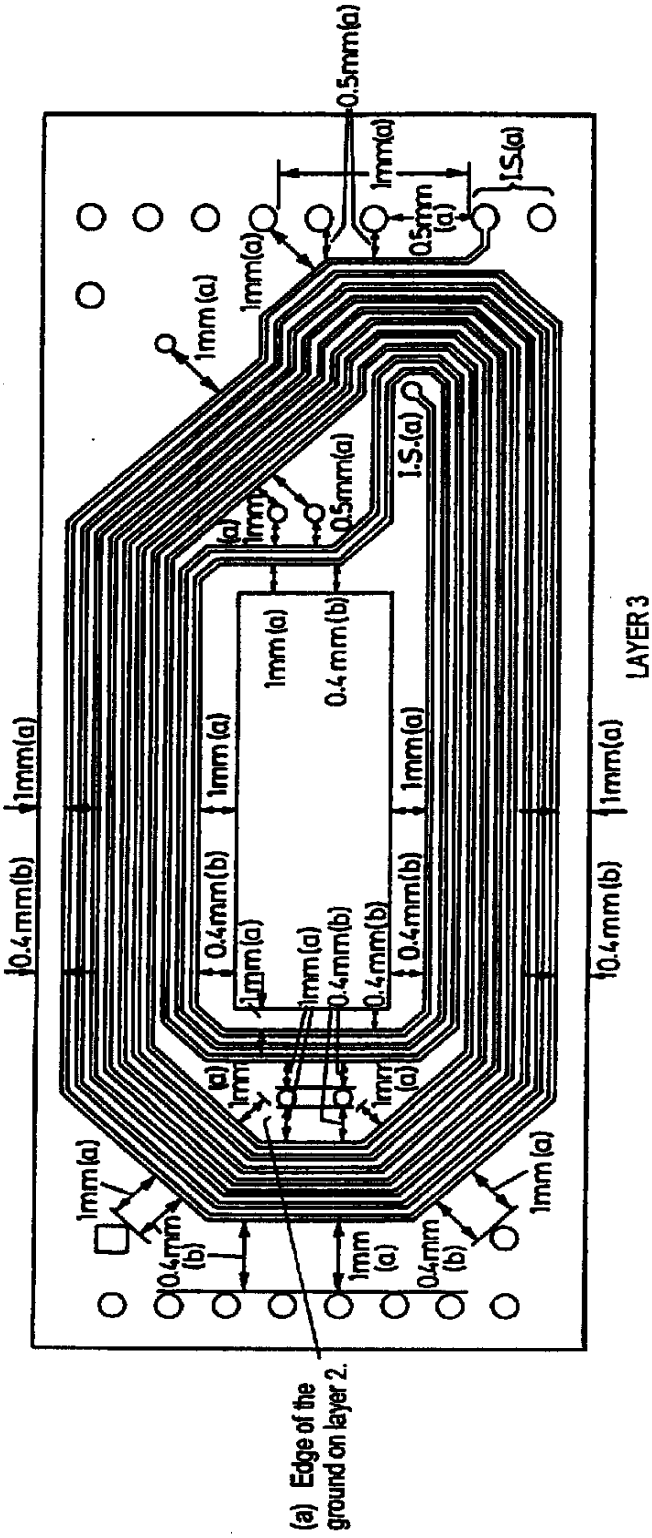

0.5mm(a)
1mm(a)
1.S.(a)
0.5mm (a)
1mm(a)
1mm (a)
1.S.(a)
0.5mm(a)
1mm (a)
0.4 mm(b)
1mm(a)
1mm (a)
1mm(a)
1mm(a)
0.4mm(b)
0.4mm(b)
1mm(a)
1mm(a)
0.4mm(b)
0.4mm(b)
1mm(a)
1mm(a)
1mm(a)
0.4mm (b)
1mm (a)
0.4mm (b)
(a) Edge of the ground on layer 2.
LAYER 3

FIG. 9

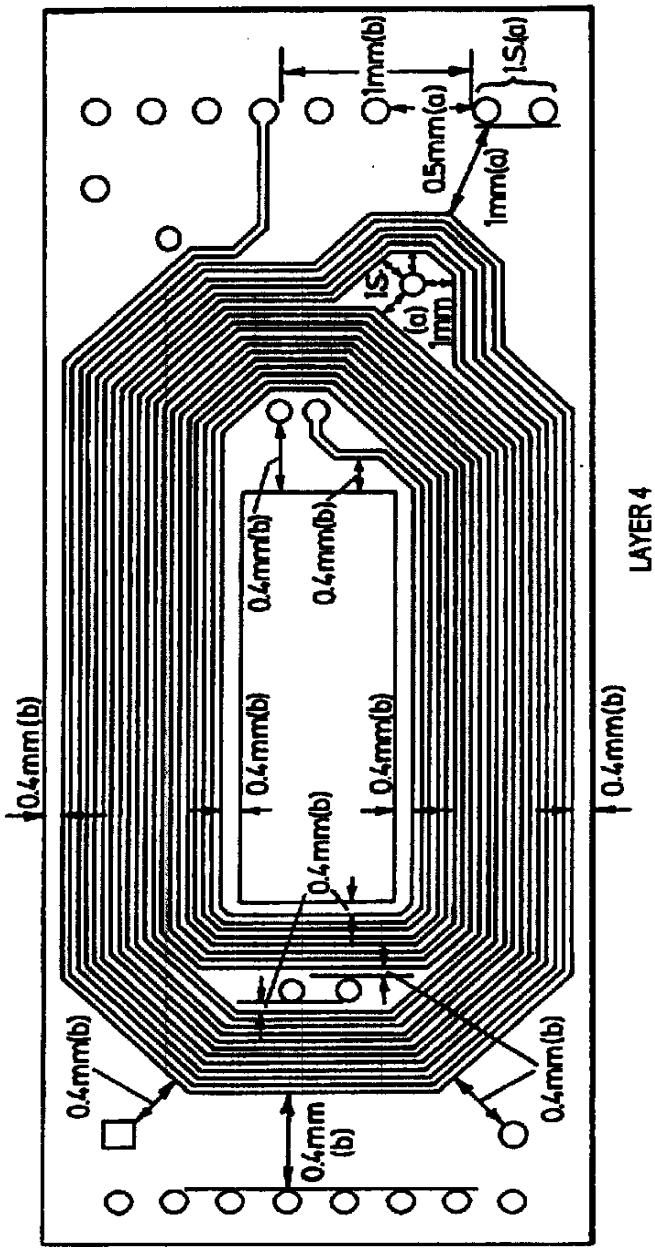

1mm(b)
1.5(a)
0.5mm(a)
1mm(a)
1.5
(a)
1mm
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm
(b)
LAYER 4

FIG. 10

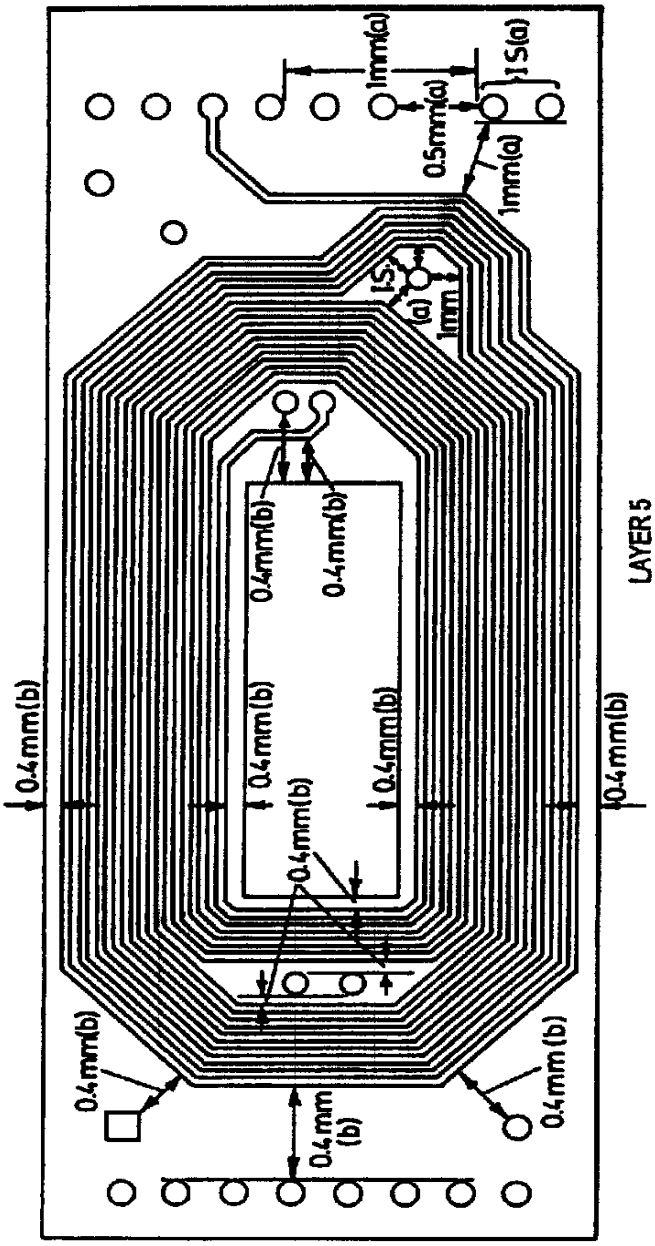

1mm(a)
1S(a)
0.5mm(a)
1mm(a)
1S
(a)
1mm
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
LAYER 5

FIG. 11

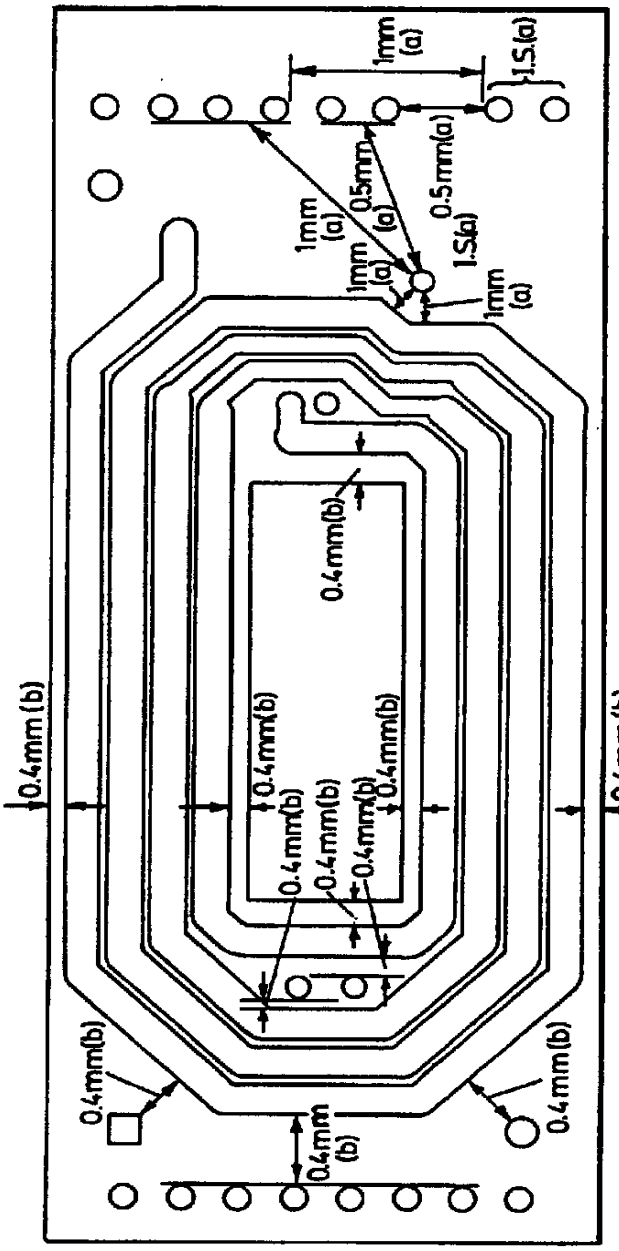

1mm (a)
1.5(a)
0.5mm(a)
0.5mm (a)
1.5(a)
1mm (a)
1mm (a)
1mm (a)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm (b)
LAYER 6

FIG. 12

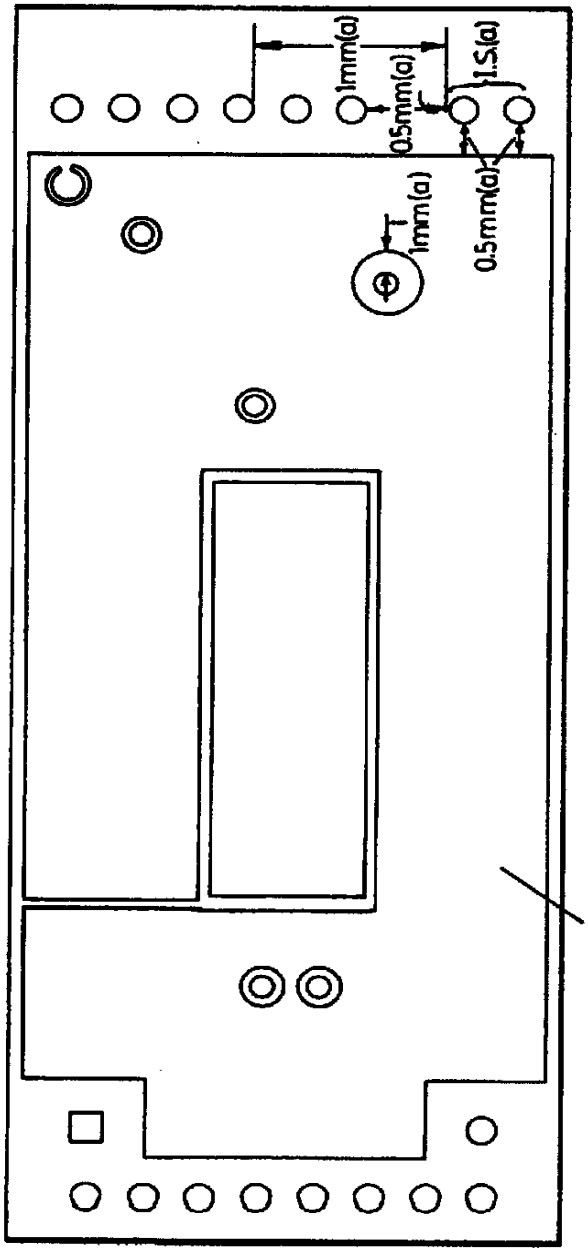

1mm(a)
0.5mm(a)
1.5(a)
1mm(a)
0.5mm(a)
LAYER 7
(b) This is not an I.S. ground (1/2 Oz only)
but it withstands 30 amperes for safety.

FIG. 13

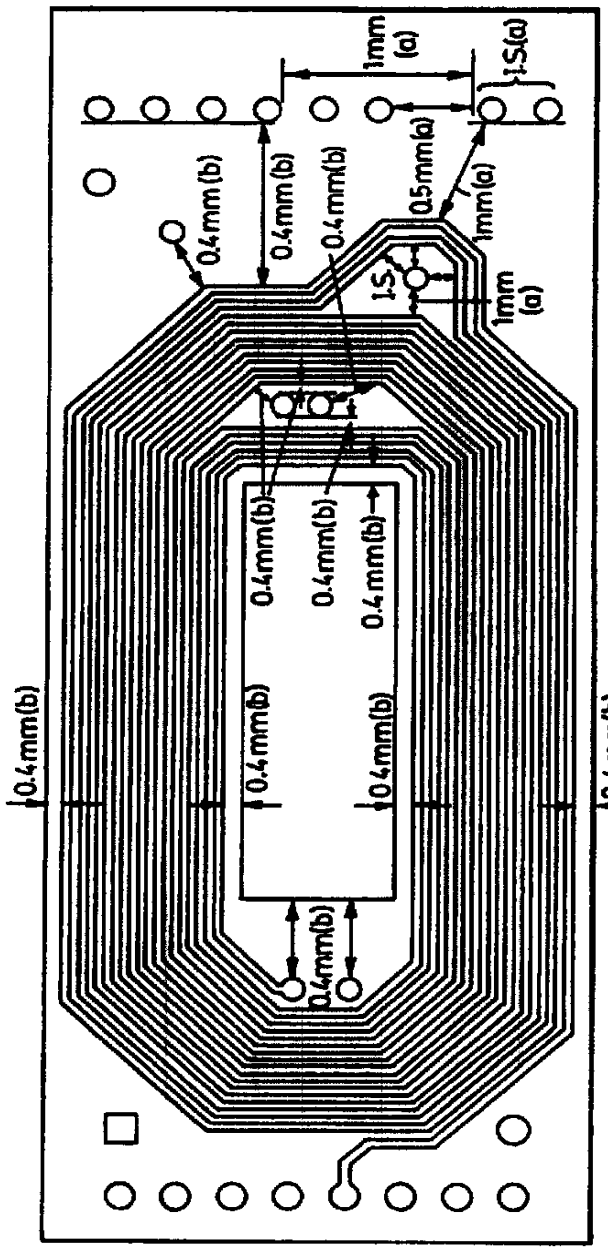

1mm (a)
1.5(a)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.5mm(a)
1mm(a)
1.5
1mm (a)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
LAYER 8

FIG. 14

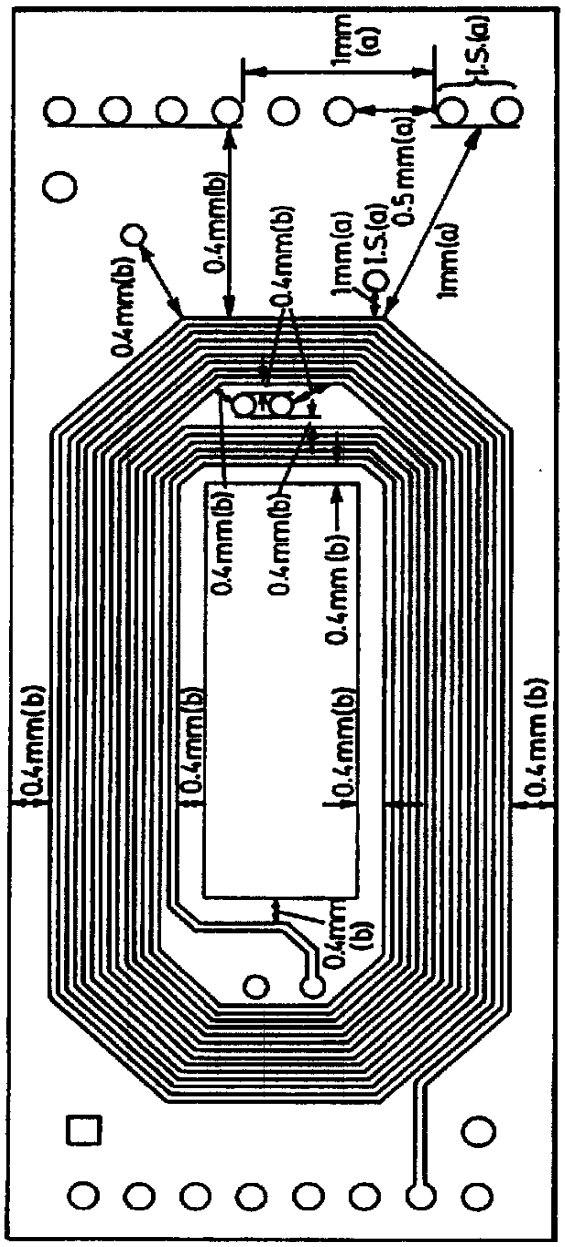

1mm (a)
1.5 (a)
0.5mm(a)
0.4mm(b)
0.4mm(b)
1mm(a)
1.5(a)
1mm(a)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm(b)
0.4mm (b)
0.4mm (b)
LAYER 9

FIG. 15

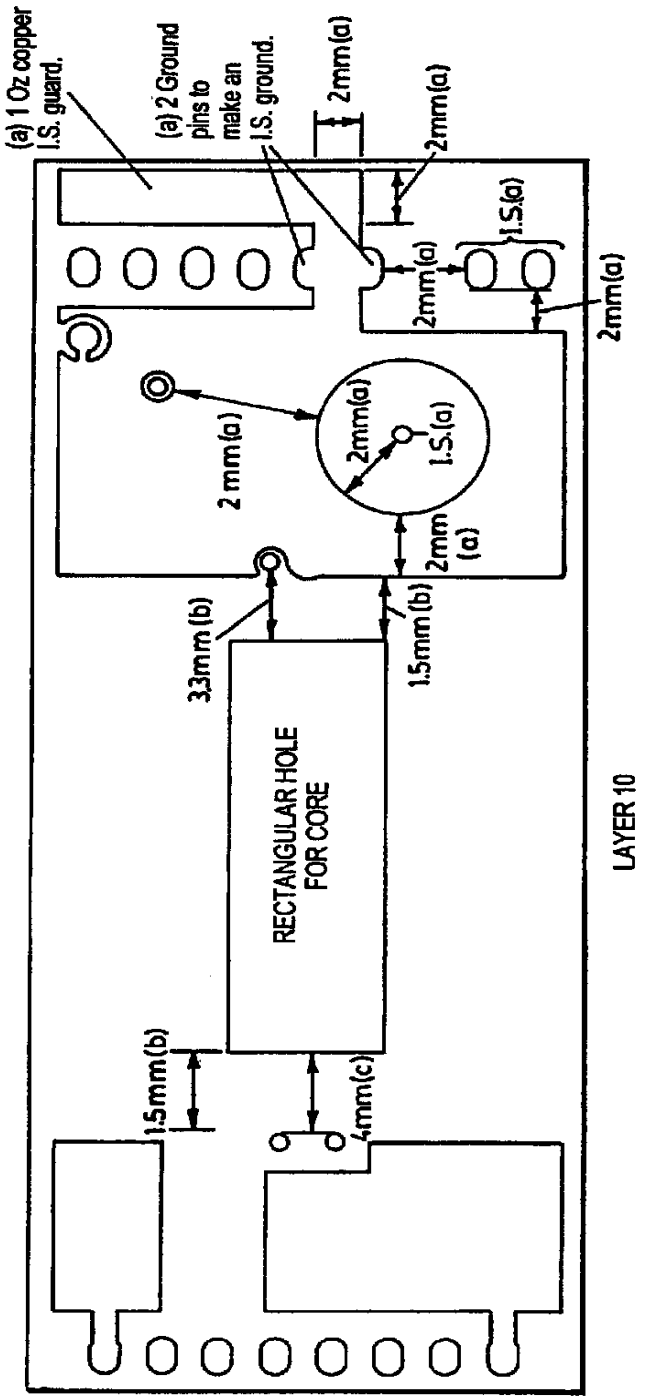

(a) 1 Oz copper I.S. guard.
(a) 2 Ground pins to make an I.S. ground.
2mm(a)
2mm(a)
I.S.(a)
2mm(a)
2mm(a)
2mm(a)
I.S.(a)
2 mm(a)
2mm (a)
3.3mm (b)
1.5mm (b)
RECTANGULAR HOLE FOR CORE
1.5mm(b)
4mm(c)
LAYER 10

FIG. 16

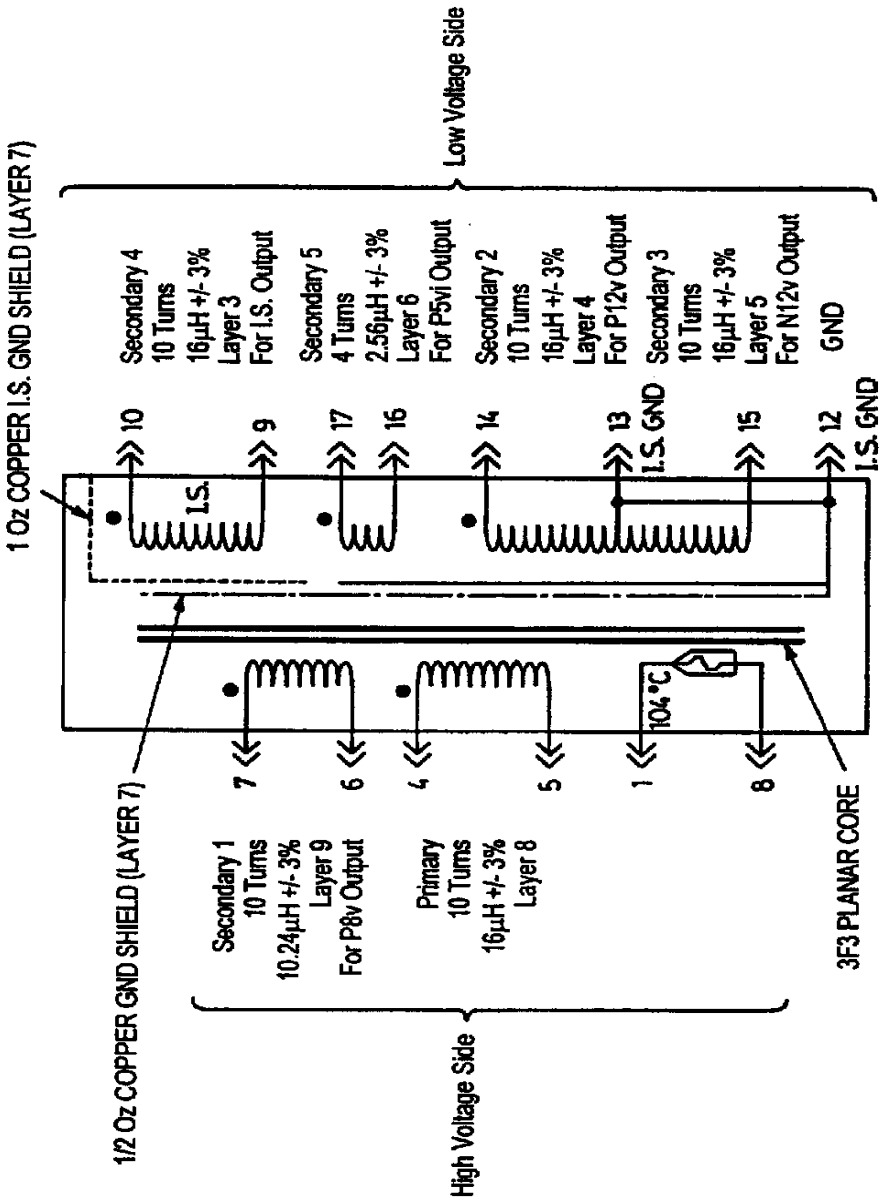

Low Voltage Side
1 Oz COPPER I.S. GND SHIELD (LAYER 7)
Secondary 4
10 Turns
16µH +/- 3%
Layer 3
For I.S. Output
Secondary 5
4 Turns
2.56µH +/- 3%
Layer 6
For P5vi Output
Secondary 2
10 Turns
16µH +/- 3%
Layer 4
For P12v Output
Secondary 3
10 Turns
16µH +/- 3%
Layer 5
For N12v Output
GND
I.S. GND
I.S.
10
9
17
16
14
13
15
12
104 °C
7
6
4
5
1
8
1/2 Oz COPPER GND SHIELD (LAYER 7)
Secondary 1
10 Turns
10.24µH +/- 3%
Layer 9
For P8v Output
Primary
10 Turns
16µH +/- 3%
Layer 8
3F3 PLANAR CORE
High Voltage Side

FIG. 17

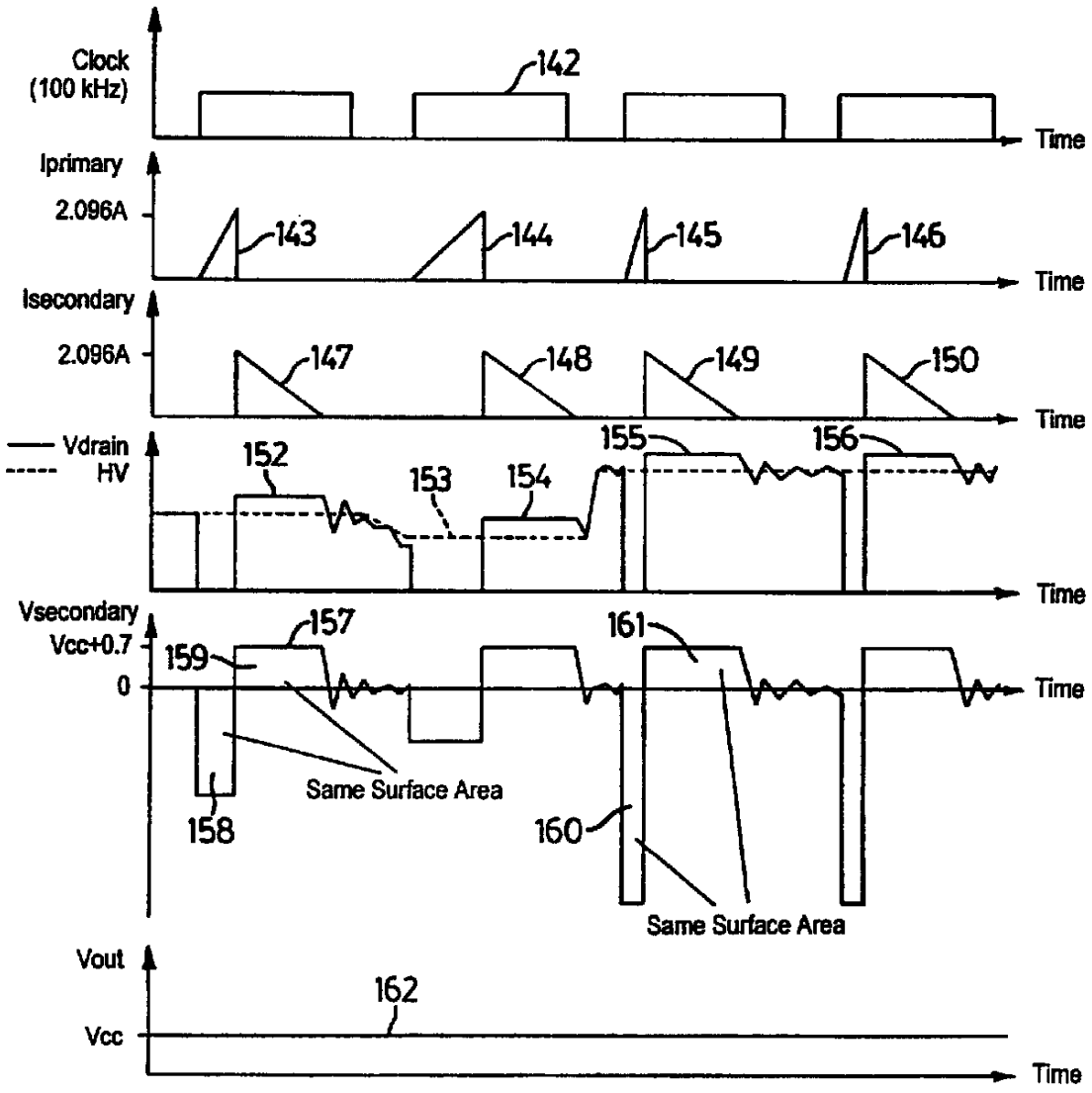

Clock
(100 kHz)
142
Time
Iprimary
2.096A
143
144
145
146
Time
Isecondary
2.096A
147
148
149
150
Time
Vdrain
HV
152
153
154
155
156
Time
Vsecondary
Vcc+0.7
0
157
159
161
Time
Same Surface Area
158
160
Same Surface Area
Vout
162
Vcc
Time

FIG. 18

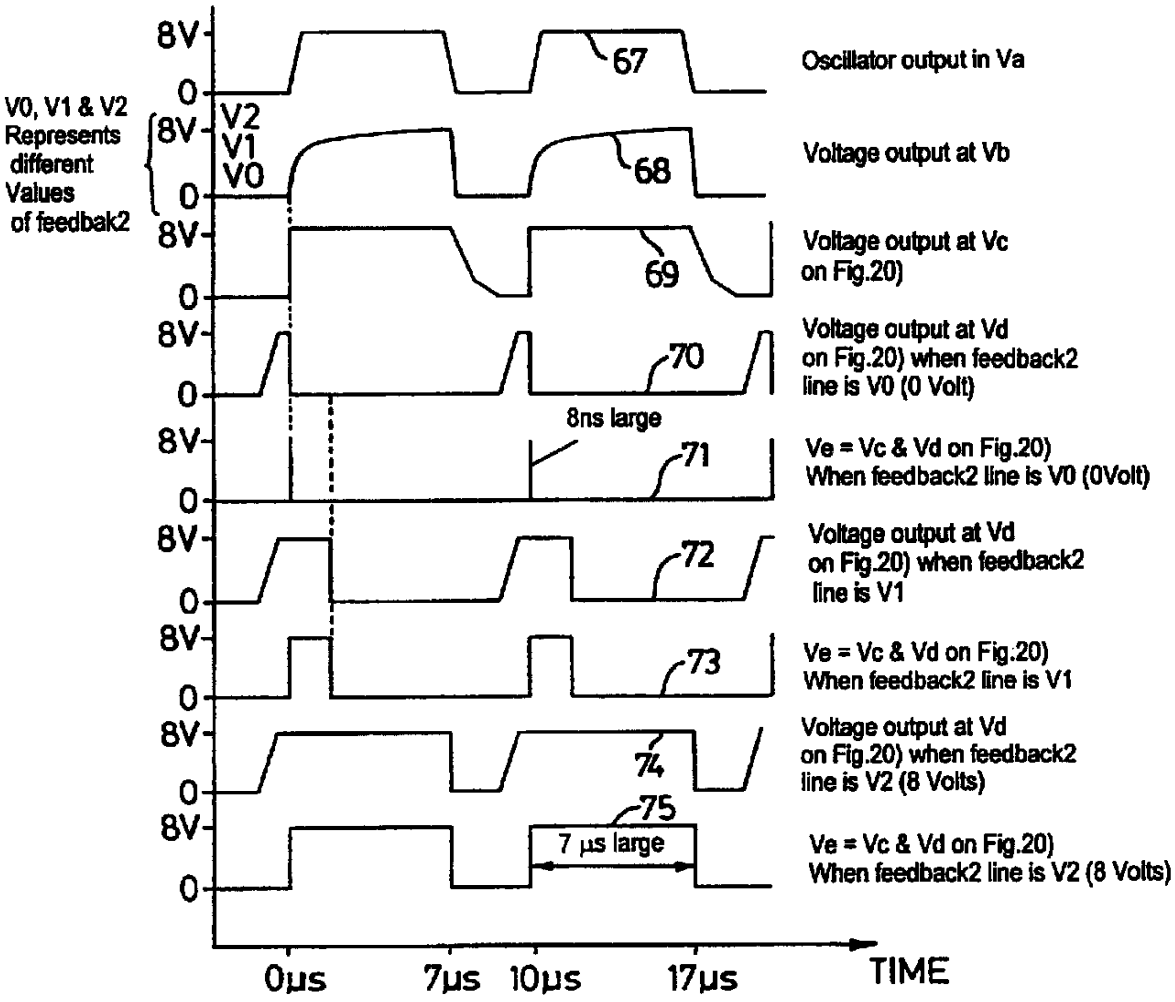

8V
0
67
Oscillator output in Va
V0, V1 & V2
Represents
different
Values
of feedbak2
V2
V1
V0
68
Voltage output at Vb
69
Voltage output at Vc
on Fig.20)
70
Voltage output at Vd
on Fig.20) when feedback2
line is V0 (0 Volt)
8ns large
71
Ve = Vc & Vd on Fig.20)
When feedback2 line is V0 (0Volt)
72
Voltage output at Vd
on Fig.20) when feedback2
line is V1
73
Ve = Vc & Vd on Fig.20)
When feedback2 line is V1
74
Voltage output at Vd
on Fig.20) when feedback2
line is V2 (8 Volts)
75
7 µs large
Ve = Vc & Vd on Fig.20)
When feedback2 line is V2 (8 Volts)
0µs
7µs
10µs
17µs
TIME

FIG. 19

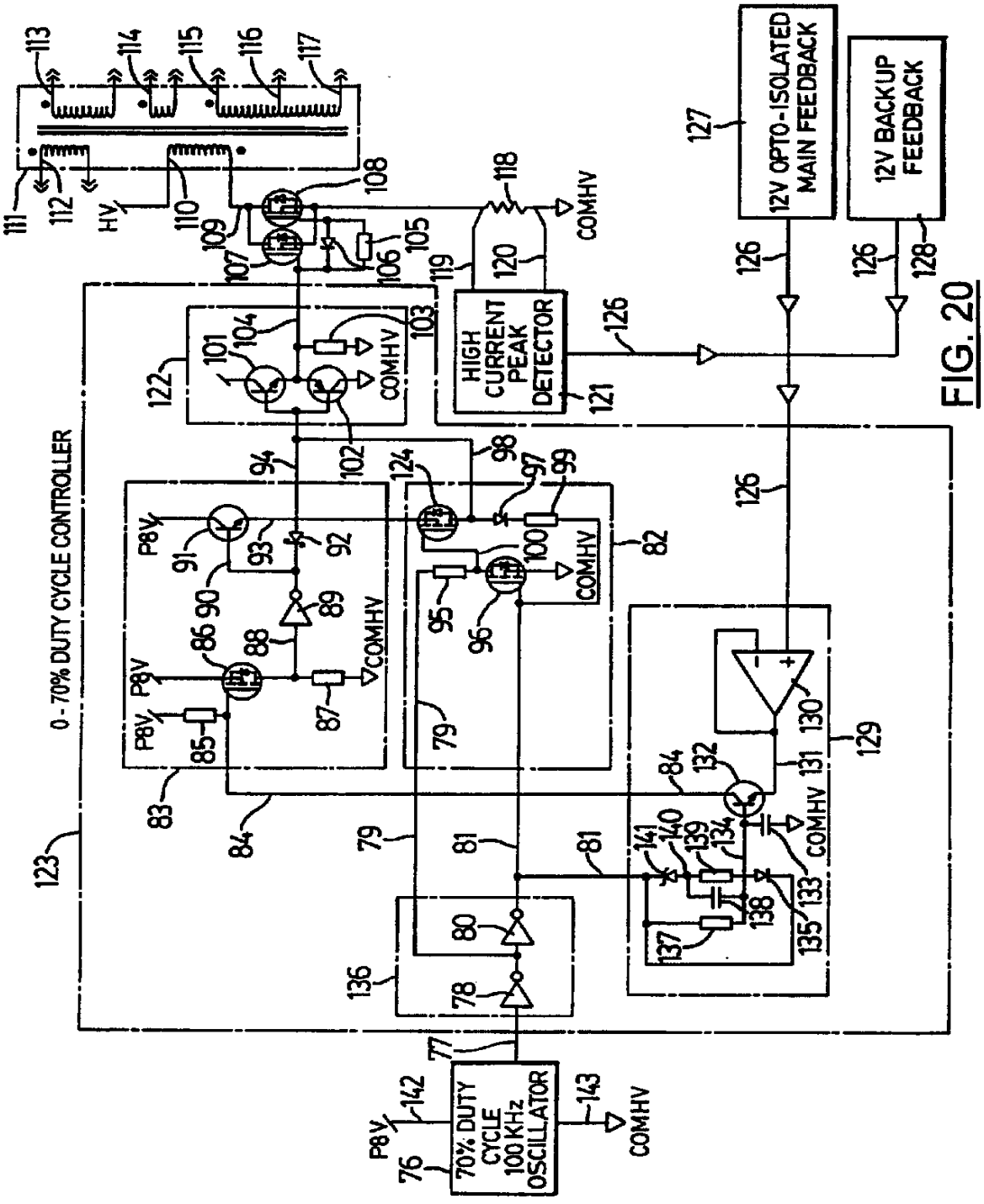

0 - 70% DUTY CYCLE CONTROLLER
12V OPTO-ISOLATED MAIN FEEDBACK
12V BACKUP FEEDBACK
HIGH CURRENT PEAK DETECTOR
70% DUTY CYCLE 100 KHz OSCILLATOR
COMHV
P8V
HV

FIG. 20

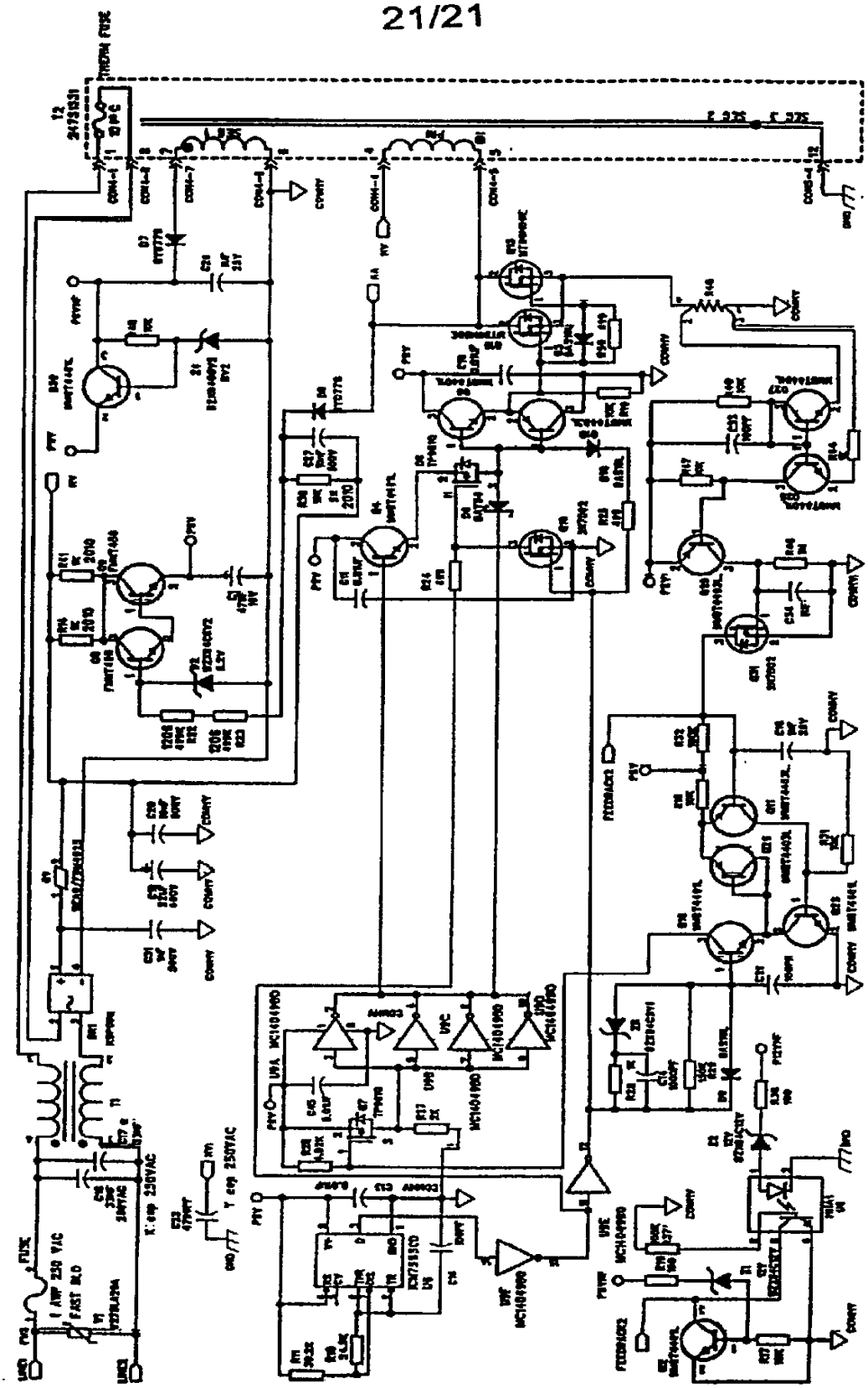


FIG. 21

INTERNATIONAL SEARCH REPORT

Interna al Application No
PCT/CA 00/00832

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H02M7/217

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 97 45946 A (HITACHI LTD.) 4 December 1997 (1997-12-04) abstract	1-3

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 August 2000	31/08/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Lund, M

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Intern al Application No
PCT/CA 00/00832

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9745946 A	04-12-1997	NONE	